AMENDMENTS TO THE SPECIFICATION

Please amend the third paragraph on page 1 as follows:

The display of an image on screen, according to usual standards, is obtained by the display of a frame or of two successive frames. Upon display of a frame, the addressing of an array screen is performed row after row via a row control circuit (commonly called the row driver). In the case of an array screen with diodes, the row electrode of the active row may be grounded while the other row electrodes may be left at high impedance or be connected to a high voltage. Simultaneously, the information corresponding to the activation or to the non-activation of the row pixels will be transmitted by the column electrodes via a column control circuit (column driver) which injects or ~~not~~ does not inject a current into each electrode column to turn on or to not turn on the column pixel.

Please amend the paragraph beginning on page 5, line 31 as follows:

It is desirable for the frame display frequency to remain substantially constant whatever the number of rows of screen 10 activated upon display of a frame. For this purpose, before display of a frame, decision unit 30 transmits to a conversion unit 36 a signal indicating which are the K "active" blocks. Conversion unit 36 determines a multiplicative factor by which the frequency of a clock signal I_{CLK} internal to the display device must be multiplied to obtain the adequate frequency of read clock signal R_{CLK} for the frequency of frame clock signal F_{CLK} to be substantially constant. Conversion unit 36 transmits the value of the multiplicative factor to a row counter 38 which provides, based on internal control signal I_{CLK}, read clock signal R_{CLK}. Read clock signal R_{CLK} is especially transmitted to counter 34 and to reading interface 24. Read clock signal R_{CLK} is also transmitted to a frame counter 40 which provides frame clock signal F_{CLK}.

Please amend the third full paragraph on page 6 as follows:

~~Reading~~ Writing interface 22 is connected to auxiliary memory 28 which is not linked to main memory 20. Each time writing interface 22 sets to 1 a memory point 19 of a row of main memory 20, it transmits to auxiliary memory 28 a signal so that the memory point of auxiliary

memory 28 associated with said row is set to 1. In the case where writing interface 22 sets a memory point of main memory 20 to 0, no signal is transmitted to auxiliary memory 28.